Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.014”**



**B**

**E**

**.014”**

**Top Material: Al**

**Backside Material: Au**

**Base = .004” X .004”**

**Emitter = .0055” X .0055”**

**Backside Potential: Collector**

**Mask Ref: CP788X**

**APPROVED BY: DK DIE SIZE .014” X .014” DATE: 10/6/21**

**MFG: CENTRAL SEMI THICKNESS .006” P/N: 2N3799**

**DG 10.1.2**

#### Rev B, 7/19/02